METHODS AND SYSTEMS FOR IMPROVING ESD CLAMP RESPONSE TIME

ABSTRACT OF THE DISCLOSURE

The present invention relates to electrostatic discharge (ESD) protection and, more particularly, to methods and systems for improving response times of ESD triggering and clamping circuitry. An ESD protection circuit protects ESD circuitry from direct current (DC) voltage stress during normal operations by reducing terminal pad voltage level. A frequency bypass circuit implemented across an ESD protection circuit essentially acts as a short circuit during ESD events and essentially acts as an open circuit during normal operations. A frequency bypass circuit implemented in conjunction with an ESD protection circuit enables ESD triggering and clamping circuitry to react to ESD events without undue delay. Unlike an ESD protection circuit, a frequency bypass circuit does not result in substantial voltage reduction across its terminals. In an embodiment, the frequency bypass circuit includes one or more capacitors. For example, in an embodiment, the frequency bypass circuit is implemented as one or more discreet capacitors and/or one or more transistor-based capacitors.